AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A semiconductor integrated device comprising a ROM decoder of n bits for selecting one gradation voltage out of gradation voltages of the n-th power of 2 gradation in connection with data signals of n bits (n represents an integer of 2 or more) representing a gradation level, said ROM decoder having n pairs of confronting gate wires each into which the data signal is input with the non-inverted state on one of the pair and with the inverted state on another of the pair,

wherein pairs of the n-th power of 2 each of which comprises an enhancement type transistor and a depletion type transistor kept under ON-state are arranged at predetermined positions one side by one side at the pair of the confronting gate wires, and with respect to each of the pair of the confronting gate wires, the width of the gate wire that contains the upper portion of the depletion type transistor and extends from the depletion type transistor to the enhancement type transistor adjacent to the depletion type transistor is reduced with respect to the width of the gate wire than contains the upper portion of the adjacent enhancement type transistor so that

recess portions are formed inside the confronting gate wires with the width of the gate wire that contains the upper portion of the depletion type transistor being narrower than the width of the gate wire than contains the upper portion of the adjacent enhancement type transistor.

2. (previously presented) The semiconductor integrated circuit device according to claim 1, wherein the width of the gate wire that contains the upper portion of the depletion type transistor and extends from the depletion type transistor to the position between the depletion type transistor and the enhancement type transistor adjacent to the depletion type transistor is reduced so that recess portions are formed inside the confronting gate wires.

3. (original) The semiconductor integrated circuit device according to claim 1, wherein with respect to each of the pair of the confronting gate wires, the width of the gate wire between continuously-arranged depletion type transistors is reduced so that recess portions are formed inside the confronting gate wires.

4. (original) The semiconductor integrated circuit device according to claim 2, wherein with respect to each of the pair of the confronting gate wires, the width of the gate wire between continuously-arranged depletion type transistors is reduced so that recess portions are formed inside the confronting gate wires.

5. (original) The semiconductor integrated circuit device according to claim 1, wherein the reduced width of the gate wire is equal to a half of the gate wire width on the enhancement type transistor.

6. (original) The semiconductor integrated circuit device according to claim 2, wherein the reduced width of the gate wire is equal to a half of the gate wire width on the enhancement type transistor.

7. (original) A liquid display device comprising the semiconductor integrated circuit device according to claim 1.

8. (original) A liquid display device comprising the semiconductor integrated circuit device according to claim 2.

9-13. (canceled)

14. (new) A semiconductor integrated device, comprising:

an n-bits ROM decoder for selecting one gradation voltage out of plural gradation voltages in connection with data signals of n bits representing a gradation level,

said ROM decoder having pairs of confronting gate wires connected to input into each pair the data signals with a non-inverted state on one of the pair and with an inverted state on another of the pair,

each pair of confronting gate wires corresponding to plural enhancement type transistors and depletion type transistors,

a first width of the gate wire that contains an upper portion of the depletion type transistor being narrower than a second width of the gate wire than contains an upper portion of an adjacent enhancement type transistor such at a recess is formed within the gate wire between two enhancement type transistors.

15. (new) The semiconductor integrated circuit device according to claim 14, wherein the first width of the gate wire of the depletion type transistor is equal to a half of the second width on the enhancement type transistor.

16. (new) The semiconductor integrated circuit device according to claim 14, wherein an overall width of the pair of confronting gate wires is twice the second width.

17. (new) A semiconductor integrated device, comprising:

a ROM decoder for selecting one gradation voltage out of plural gradation voltages in connection with data signals of n bits representing a gradation level,

said ROM decoder having pairs of confronting gate wires connected to input into each pair the data signals with a non-inverted state on one of the pair and with an inverted state on another of the pair,

each gate wire having a first width over an upper portion of the depletion type transistor and a second width over an upper portion of an adjacent enhancement type transistor, the

first width being less than the second width such at a recess is formed in the gate wire between two enhancement type transistors.

18. (new) The semiconductor integrated circuit device according to claim 17, wherein the first width of the gate wire over the depletion type transistor is equal to a half of the second width of the gate wire over the enhancement type transistor.

19. (new) The semiconductor integrated circuit device according to claim 17, wherein an overall width of the pair of confronting gate wires is twice the second width.

20. (new) The semiconductor integrated circuit device according to claim 18, wherein an overall width of the pair of confronting gate wires is twice the second width.